



Sheet 1 of 1

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

58269.00003

SERIAL NO.

09/827,175

LIST OF REFERENCES CITED BY APPLICANT

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SOKOL et al.

FILING DATE

April 6, 2001

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						

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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO PART.		
	AG	WO 97/50214	December 31, 2003	WIPO			X		
	AH								
	AI								
	AJ								
	AK								

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	AL	W.E. Denzel, A.P.J. Engbersen, I. Iliadis: "A Flexible Shared-Buffer Switch for ATM at Gb/s Rates"; Computer Networks and ISDN Systems, North Holland Publishing, Amsterdam, NL; vol. 27, No. 4, 1995, pages 611-624; XP000600212; ISSN 0169-7552
	AM	Liang-Teh Lee, Po-Hsian Huang: "A High Speed Factorial Style Memory Switch"; IEICE Transactions on Communications, Institute of Electronics Information and Comm. Eng., Tokyo, Japan, Vol. E81-B, No. 2, 1 February 1998 (1998-02-01), pages 164-174, XP000778251; ISSN 0916-8516
	AN	

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Sheet 1 of 3

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
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ATTY. DOCKET NO.

023925-00003

SERIAL NO.

09/827,175

LIST OF REFERENCES CITED BY APPLICANT

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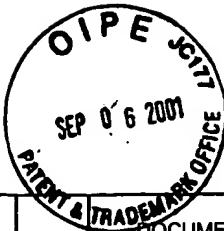
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KM	AA	5,555,398	Sep. 10, 1996	Raman			Apr. 15, 1994
	AB	5,644,784	Jul. 1, 1997	Peek			Mar. 3, 1995
	AD	5,828,653	Oct. 27, 1998	Goss			Apr. 26, 1996
	AE	5,423,015	Jun. 6, 1995	Chung			May 21, 1991
	AF	5,696,899	Dec. 9, 1997	Kalwitz			Nov. 18, 1992
	AG	6,061,351	May 9, 2000	Erimli et al.			Dec. 18, 1997
	AH	5,748,631	May 5, 1998	Bergantino et al.			May 9, 1996
	AI	6,119,196	Sep. 12, 2000	Muller et al.			Jun. 30, 1997
	AJ	6,175,902 B1	Jan. 16, 2001	Runaldue et al.			Dec. 18, 1997
	AK	5,473,607	Dec. 5, 1995	Hausman et al.			Aug. 9, 1993
	AL	5,787,084	Jul. 28, 1998	Hoang et al.			Jun. 5, 1996
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	AR	5,524,254	Jun. 4, 1996	Morgan et al.			Jul. 1, 1994
	AS	5,987,507	Nov. 16, 1999	Creedon et al.			Dec. 29, 1998
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	AU	5,781,549	Jul. 14, 1998	Dai			Feb. 23, 1996
	AV	6,041,053	Mar. 21, 2000	Douceur et al.			Sep. 18, 1997
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	BA	5,414,704	May 9, 1995	Spinney			Apr. 5, 1994
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<i>KMG</i>	BE	5,918,074	Jun 29, 1999	Wright et al.			Jul. 25, 1997
	BF	5,898,687	Apr. 27, 1999	Harriman et al.			Jul. 24, 1996
	BG	5,940,596	Aug. 17, 1999	Rajan et al.			Aug. 4, 1997
	BH	5,802,052	Sep. 1, 1998	Venkataraman			Jun. 26, 1996
	BI	5,842,038	Nov. 24, 1998	Williams et al.			Oct. 10, 1996
	BJ	5,742,613	Apr. 21, 1998	MacDonald			Apr. 27, 1993
	BK	5,579,301	Nov. 26, 1996	Ganson et al.			Feb. 28, 1994
	BL	5,278,789	Jan. 11, 1994	Inoue et al.			Dec. 6, 1991
	BM	5,652,579	Jul. 29, 1997	Yamada et al.			Aug. 15, 1996
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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO PART.		
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	BP	EP0465090A1	Jan. 8, 1992	EPO					
	BQ	EP0859492A2	Aug. 19, 1998	EPO					
	BR	EP0312917A2	Apr. 26, 1989	EPO					
	BS	EP0853441A2	Jul. 15, 1998	EPO					
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	BW	EP0862349A2	Sep. 2, 1998	EPO					Abs
	BX	FR 2 725 573 - A1	Apr. 12, 1996	France					Abs
	BY	EP0854606A2	Jul. 22, 1998	EPO					
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	CG	EP0849917A2	Jun. 24, 1998	EPO					
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	CI	"A High-Speed CMOS Circuit for 1.2-Gb/s 16 x 16 ATM Switching," Alain Chemarin et al. 8107 IEEE Journal of Solid-State Circuits 27(1992) July, No. 7, New York, US, pages 1116-1120
	CJ	"Local Area Network Switch Frame Lookup Technique for Increased Speed and Flexibility," IBM Technical Disclosure Bulletin 38(1995) July, No. 7, Armonk, NY, US, pages 221-222
	CK	"Queue Management for Shared Buffer and Shared Multi-buffer ATM Switches," Yu-Sheng Lin et al. Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C., March 24, 1996, pages 688-695
	CL	"A 622-Mb/s 8 x 8 ATM Switch Chip Set with Shared Multibuffer Architecture," Harufusa Kondoh et al., 8107 IEEE Journal of Solid-State Circuits 28(1993) July, No. 7, New York, US, pages 808-814
	CM	"Catalyst 8500 CSR Architecture," White Paper XP-002151999, Cisco Systems Inc. 1998, pages 1-19
	CN	"Computer Networks," A.S. Tanenbaum, PRENTICE-HALL INT., USA, XP-002147300(1998), Sec. 5.2-Sec. 5.3, pages 309-320

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